

**EAST Search History****EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	6006	716/2,6,11.ccls.	US_PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 18:03
L2	40	@ad<"20031128" and ( (determin\$5 find\$3 ascertain\$4 detect\$3 collect\$3 discover\$3 establish\$3 identif\$7) with (clock "clk" "ck") with (delay) with (plural\$4 multiple all different\$3 each second third\$3) ) and ( (allocat\$3 assign\$4 allot\$5 budget\$3 designat \$3 earmark\$3) with (clock "clk" "ck") ) and ( (optim \$7 with (time timing)) ) and (layout)	US_PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/10 18:10
S2	11	((determin\$5 ascertain\$3 detect\$3 assess\$3 evaluat \$3 calculat\$3) near number\$3 near5 (clock\$3 timer\$2) with ((differ\$3 dissimilar deviat\$3 inconsistent unequal unsimilar unalike distinct \$5) with (delay\$3))) and @ad<"20041128"	US_PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/12 00:17
S3	375	(determin\$5 ascertain\$3 detect\$3 assess\$3 evaluat \$3 calculat\$3) with number\$3 with (clock\$3 timer\$2) same ((differ\$3 dissimilar deviat\$3 inconsistent unequal unsimilar unalike distinct \$5) with (delay\$3))	US_PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/12 00:48

S4	40	@ad< "20031128" and ( (determin\$5 find\$3 ascertain\$4 detect\$3 collect\$3 discover\$3 establish\$3 identif\$7) with (clock "clk" "ck") with (delay) with (plural\$4 multiple all different\$3 each second third\$3) ) and ( (allocat\$3 assign\$4 allot\$5 budget\$3 designat\$3 earmark\$3) with (clock "clk" "ck") ) and ( (optim\$7 with (time timing)) ) and (layout)	US_PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/12 01:28
S5	23	@ad< "20031128" and ( (clock "clk" "ck" tree path) with (delay) near4 (different\$3 varying varies vary) ) and ( (allocat\$3 assign\$4 allot\$5 budget\$3 designat\$3 earmark\$3 distribut\$3) with (clock "clk" "ck") ) and (optim\$7 with (timing time tree clock "clk" "ck")) and ((clock "clk" "ck" tree) with (synthesis translation)) and layout	US_PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/12 01:53
S6	72	@ad< "20031128" And ( netlist ( ((gate adj level) netlist rtl hdl verilog vhdl logic\$2) adj (stage phase design routine) ((clock buffer) near4 (skeleton synthesis tree)) ((clock buffer) near2 (tree distribution) near2 (synthesiz\$7 build\$3 produc\$4 generat\$4 creat\$4)) ) with ( (timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice) ) And ( layout same ( (timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 driven based)) sta spice) ) And Delay And Skew\$3 And ( (clock timing buffer) with (spec specification configuration requirement definition defin\$3 character\$7	US_PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/12 02:49

		constraint goal) or ( (identify\$7 determin\$5 calculat\$4 ascertain\$5 list \$3 report\$3) with (clock near (net source domain structure element block need\$4 used utili\$7) ) And (clock buffer) with (allocat\$4 defin\$5 generat \$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3 apportion\$3 asign\$5)				
S10	423	@ad<"20031128" and delay and skew and ((logic circuit functional (front near2 end) with (phase stage design\$3 process\$3 routine)) and ((physical layout (back near2 end)) with (phase stage design\$3 process\$3 routine)) and ((number value) with (clock tree buffer driver repeater)) and (sta or ((time timing transient spice) near3 (analy\$7)) )	US_PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/12 03:21
S11	238	@ad<"20031128" And ( (technology near independent) (front adj end) functional rtl hdl ((gate near level) near (specification description)) netlist (logic \$2 near2 (phase stage design\$3 process\$3 routine)) ) with ( (timing near5 (analy\$5 closure converg\$5 verif\$5 optim \$7 check\$4 static validat \$3)) sta spice) And ( (technology near dependent) (back adj end) layout (physical near2 (phase stage design \$3 process\$3 routine)) ) with ( (timing near5 (analy \$5 closure converg\$5 verif \$5 optim\$7 check\$4 static validat\$3)) sta spice) And (clock timing buffer) with (spec specification configuration requirement definition defin\$3)	US_PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/12 03:46

S12	238	<p>@ad&lt;"20031128" And</p> <p>((technology near independent) (front adj end) functional rtl hdl ((gate near level) near (specification description)) netlist (logic \$2 near2 (phase stage design\$3 process\$3 routine)) ) with ( (timing near5 (analy\$5 closure converg\$5 verif\$5 optim \$7 check\$4 static validat \$3) sta spice) And</p> <p>((technology near dependent) (back adj end) layout (physical near2 (phase stage design \$3 process\$3 routine)) ) with ( (timing near5 (analy \$5 closure converg\$5 verif \$5 optim\$7 check\$4 static validat\$3) sta spice) And</p> <p>(clock timing buffer) with (spec specification configuration requirement definition defin\$3)</p>	US_PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/12 12:24
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9/10/2010 6:14:45 PM

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